What is Claimed is:

1. A method for reducing power consumption in a programmable logic device, the programmable logic device for conducting a plurality of signals, comprising:

evaluating whether a first signal is being conducted on the lowest power wire;

if the lowest power wire is being used to conduct the first signal, proceeding to evaluate a second signal; and

if the lowest power wire is not being used to conduct the first signal, determining the lowest power wire upon which the first signal can be conducted in view of other considerations including at least one of programmable logic device speed and programmable logic device routability.

2. The method of claim 1, wherein the evaluating occurs during a synthesis period relating to the first signal.

3. The method of claim 1, wherein the evaluating occurs during a placement period relating to the first signal.

4. The method of claim 1, wherein the evaluating occurs during a routing period relating to the first signal.

5. The method of claim 1, further comprising determining the change in speed of a function associated with the first signal, the change

in speed that is attributable to a change of routing to the lowest power wire.

6. The method of claim 1, further comprising determining the change in routing density of the routing associated with the first signal and the associated routing, the change in routing density that is attributable to routing the first signal to the lowest power wire.

7. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of logic elements, the method comprising:

evaluating whether a first logic element is used for a design implemented in the programmable logic device;

if the first logic element is used for the design, evaluating a second logic element;

if the first logic element is not used for the design, determining the state of the output of the first logic element that causes the programmable logic device to consume the least power; and

where a programmable logic device speed specification and a programmable logic device routability specification permit, setting the state of the output of the first logic element to the state that causes the programmable logic device to consume the least power.

8. The method of claim 7, wherein the evaluating occurs during a synthesis period relating to the first logic element.

9. The method of claim 7, wherein the evaluating occurs during a routing period relating to the first logic element.

10. The method of claim 7, wherein the evaluating occurs following a routing period relating to the first logic element.

11. The method of claim 7, wherein the evaluating occurs during a placement period relating to the first logic element.

12. The method of claim 7, further comprising determining the change in speed of a function associated with the first logic element, the change in speed that is attributable to the setting.

13. The method of claim 7, further comprising determining the change in area of the first logic element and the associated routing, the change in area that is attributable to the setting.

14. The method of claim 7, the setting comprising increasing a number of transistors associated with the logic element that have substantially no voltage differential between a source and a drain.

15. The method of claim 7, wherein the setting the state of the output of the first logic element to the state that causes the programmable logic

device to consume the least power comprises finding and routing a signal into the first logic element.

16. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of logic array blocks, each of the logic array blocks that comprises multiplexers and a plurality of logic elements, at least one of the logic array blocks being active, the method comprising:

evaluating whether a first logic array block is used for the design;

if the first logic array block is used for the design, evaluating whether the functions of the first logic element can be allocated to the active logic array block;

if the first logic array block is not used for the design, proceeding to evaluate a second logic array block; and

when the functions of the first logic element can be allocated to the active logic array block and when a programmable logic device speed specification and a programmable logic device routability specification permit, allocating the functions of the first logic array block to the active logic array block.

17. The method of claim 16, wherein the evaluating whether a first logic array block is used for the design occurs during a synthesis period relating to the first logic array block.

18. The method of claim 16, wherein the evaluating whether a first logic array block is used for the design occurs during a routing period relating to the first logic array block.

19. The method of claim 16, wherein the evaluating whether a first logic array block is used for the design occurs following a routing period relating to the first logic array block.

20. The method of claim 16, further comprising determining the change in speed of a function associated with the first logic array block, the change in speed that is attributable to the allocating.

21. The method of claim 16, wherein the evaluating whether a first logic array block is used for the design occurs during a placement period relating to the first logic array block.

22. The method of claim 16, further comprising determining the change in routing associated with the active logic array block, the change in routing that is attributable to the allocating.

23. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a logic region, the logic region including configuration information and logic state information, the method comprising:

for a particular time period, evaluating whether the logic state information is necessary for the operation of the programmable logic device;

if the logic state information is required for operation of the programmable logic device, maintaining the configuration information and the logic state information;

if the logic state information is not necessary, maintaining the configuration information and reducing power to the portion of the region associated with maintaining the logic state information.

24. The method of claim 23, further comprising determining the change in speed associated with the reducing power to the portion of the region associated with maintaining the logic state information.

25. The method of claim 23, further comprising determining the change in routing associated with the reducing power to the portion of the region associated with maintaining the logic state information.

26. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a logic region, the logic region including configuration information and logic state information, the method comprising:

during operation of the programmable logic device, evaluating whether the logic state information is necessary for a particular time period;

if the logic state information is necessary, maintaining the configuration information and the logic state information;

if the logic state information is not necessary, maintaining the configuration information and reducing power to the portion of the region associated with maintaining the logic state information.

27. The method of claim 26, further comprising determining the change in speed associated with the reducing power to the portion of the region associated with maintaining the logic state information.

28. The method of claim 26, further comprising determining the change in routing associated with the reducing power to the portion of the region associated with maintaining the logic state information.

29. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of transistors, the method comprising:

evaluating whether a first transistor or group of transistors is used for a design implemented in the programmable logic device;

if the first transistor or group of transistors is not used for the design, evaluating a second transistor or group of transistors;

if the first transistor or group of transistors is used for the design, determining whether the first transistor or group of transistors can be reverse biased to operate in a low power mode; and

if the first transistor or group of transistors can be reverse biased to operate in a low power mode and a programmable logic device speed specification and a programmable logic device routability specification permit, reverse biasing the first transistor or group of transistors to operate in low power mode.

30. The method of claim 29, wherein the evaluating occurs during a synthesis period relating to the first transistor or group of transistors.

31. The method of claim 29, wherein the evaluating occurs during a routing period relating to the first transistor or group of transistors.

32. The method of claim 29, wherein the evaluating occurs following a routing period relating to the first transistor or group of transistors.

33. The method of claim 29, wherein the evaluating occurs during a placement period relating to the first transistor or group of transistors.

34. The method of claim 29, further comprising determining the change in speed of a function associated with the first transistor or group of transistors, the change in speed that is attributable to the reverse biasing.

35. The method of claim 29, further comprising reverse biasing all transistors in a programmable logic device region.

36. The method of claim 29, further comprising reverse biasing all transistors in a programming element.

37. The method of claim 29, further comprising dynamically reverse biasing a plurality of transistors based on signals received via an input pin.

38. The method of claim 29, further comprising utilizing at least one of synthesis programming, logic placement programming and routing programming to over-achieve timing goals in a portion of the programmable logic device in order to allow at least one transistor to be reverse biased while still meeting performance requirements for the programmable logic device.

39. The method of claim 29 further comprising grouping a plurality of signal routs into a region of the programmable logic device, the plurality of signal routs comprising transistors that may be reverse biased while maintaining the programmable logic device speed specification and the programmable logic device routability specification.

40. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a clock network, the clock network that provides clocking signals to the programmable logic device, the method comprising:

evaluating whether a portion of the clock network may be turned OFF;

if the portion of the clock network may be turned OFF, turning OFF the portion of the clock network.

41. The method of claim 40, wherein the evaluating occurs during a synthesis period relating to the programmable logic device.

42. The method of claim 40, wherein the evaluating occurs during a placement period relating to the programmable logic device.

43. The method of claim 40, wherein the evaluating occurs during a routing period relating to the programmable logic device.

44. The method of claim 40, further comprising determining a change in speed associated with the turning OFF the portion of the clock network.

45. The method of claim 40, further comprising determining a change in routing associated with the turning OFF the portion of the clock network.

46. The method of claim 40, further comprising localizing a plurality of destinations of the clock network in order to reduce the number of active clock network branches.

47. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of transistors, the method comprising:

determining whether the first transistor can be replaced by a stack of transistors in series; and

if the first transistor can be replaced by a stack of transistor in series and a programmable logic device speed specification and a programmable logic device routability specification permit, replacing the first transistor with the transistor stack.

48. The method of claim 47, wherein the determining occurs during a synthesis period relating to the first transistor.

49. The method of claim 47, wherein the determining occurs during a routing period relating to the first transistor.

50. The method of claim 47, wherein the determining occurs following a routing period relating to the first transistor.

51. The method of claim 47, further comprising determining the change in speed of a function associated with the first transistor, the change in speed that is attributable to the replacing the first transistor with the transistor stack.

52. The method of claim 47, wherein the determining occurs following a routing period relating to the first transistor.

53. The method of claim 47, wherein the determining occurs during a placement period relating to the first transistor.

54. The method of claim 47, further comprising providing a plurality of buffers including stacked transistors in order to ensure that the

programmable logic device can arrange to have two or more transistors to turn OFF.

55. The method of claim 47, further comprising providing a plurality of multiplexers including stacked transistors in order to ensure that the programmable logic device can arrange to have two or more transistors to turn OFF.

56. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of transistors, the method comprising:

evaluating whether a first transistor is used for a design implemented in the programmable logic device;

if the first transistor is not used for the design, evaluating a second transistor;

if the first transistor is used for the design, determining whether the first transistor can be reverse biased to operate in a low power mode; and

if the first transistor can be reverse biased to operate in a low power mode and a programmable logic device speed specification and a programmable logic device routability specification permit, reverse biasing the first transistor to operate in low power mode.

57. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a full speed mode and a stand-by mode, the method comprising:

determining whether the programmable logic device is in stand-by mode;

if the programmable logic device is in stand-by mode, whether a portion of the device may be turned OFF;

if the portion of the device may be turned OFF, turning OFF the portion of the device.

58. The method of claim 57, wherein the device is a router and the stand-by mode is implemented when the router is not receiving data.

59. The method of claim 57, wherein the portions of the device that are turned OFF relate to the internal logic state of the router.

60. The method of claim 57, wherein the portions of the device that are not turned OFF relate to the configuration of the router.

61. A programmable logic device according to the invention including a heterogeneous routing pool, the pool comprising:

areas of low-power routing; and

areas of high-power routing.

62. The programmable device of claim 61, where the routing pool has three or more gradations of low, medium, and high power routing resources

63. The programmable device of claim 61, where the logic cells have a heterogeneous power profile.

64. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a logic region, the logic region including configuration information and logic state information, the method comprising:

prior to or during a logic placement period of the programmable logic device, evaluating whether a portion of the programmable logic device can be powered down during operation of the programmable logic device;

if a portion of the programmable logic device can be powered down, routing logic functions that cannot be powered down to a portion of the programmable logic device different from the portion of the programmable logic device that can be powered down.

65. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of logic elements, the method comprising:

evaluating whether a first logic element is used for a design implemented in the programmable logic device;

if the first logic element is used for the design, evaluating whether that cell has a substantially equal frequency of being a zero and a one;

if the first logic element is used for the design and has an substantially equal frequency of being a zero and a one, evaluating a second logic element;

if the first logic element is not used for the design or is used and has a substantially unequal distribution of being a zero or a one, determining the state of the output of the first logic element that causes the programmable logic device to consume the least power; and

where a programmable logic device speed specification and a programmable logic device routability specification permit, setting the state of the output of the first logic element to the state that causes the programmable logic device to consume the least power.

66. The method of claim 65, wherein the evaluating occurs during a synthesis period relating to the first logic element.

67. The method of claim 65, wherein the evaluating occurs during a routing period relating to the first logic element.

68. The method of claim 65, wherein the evaluating occurs following a routing period relating to the first logic element.

69. The method of claim 65, further comprising determining the change in speed of a function associated with the first logic element, the change in speed that is attributable to the setting.

70. The method of claim 65, further comprising determining the change in area of the first logic element and the associated routing, the change in area that is attributable to the setting.

71. The method of claim 65, the setting comprising increasing a number of transistors associated with the logic element that have substantially no voltage differential between a source and a drain.

72. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claims 1 coupled to the processing circuitry and the memory.

73. A printed circuit board on which is mounted a programmable logic device as defined in claim 72.

74. The printed circuit board defined in claim 72 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

75. The printed circuit board defined in claim 72 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

76. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of multiplexers, each of

the multiplexers comprising a plurality of inputs, the method comprising:

where a programmable logic device speed specification and a programmable logic device routability specification permit, minimizing the use of multiplexers that comprise one input that switches with a substantially greater frequency than the remaining inputs; and

maximizing the occurrence of multiplexers that comprise no input that switches.

77. A programmable logic device comprising a plurality of power-down portions that may be powered down when that portion is not used by user logic.

78. The device of claim 77 where the logic cells in a region are powered down, but the routing in the region is actively powered.

79. The method of claim 77 where the power-down portions are adapted to be dynamically turned ON and OFF during chip operation, and where configuration information is maintained during power-down.

80. The method of claim 77 where user state information contained in registers is maintained during power-down.

81. A programmable logic device comprising:

a plurality of sub-regions; and

wherein a portion of the transistors in each region is adapted to be reverse-biased during configuration in order to reduce leakage current.

82. The device of claim 81, wherein a portion of the transistors in each region is adapted to be reverse-biased dynamically during programmable logic device operation.

83. The device of claim 81, wherein a portion of the transistors in each region is adapted to be forward biased to speed up the operation of the portion of transistors.

84. The device of claim 81 wherein the a portion of the transistors in each region is adapted to be forward biased during operation of the programmable logic device.

85. A programmable logic device comprising:

unused routing that is tied OFF to one of a VCC or a Ground.

86. The programmable logic device of claim 85, wherein at least one wire of the unused routing may be tied off to only one of VCC or Ground.

87. The programmable logic device of claim 85, wherein tying off of unused routing occurs during manufacturing of the programmable logic device.

88. A programmable logic device comprising:

a plurality of transistors, a portion of the transistors being stacked in series such that the transistors are configured to operate redundantly.

89. A method for increasing speed of signal propagation in a programmable logic device, the

programmable logic device comprising a plurality of transistors, the method comprising:

evaluating whether a first transistor or group of transistors is used for a design implemented in the programmable logic device;

if the first transistor or group of transistors is not used for the design, evaluating a second transistor or second group of transistors;

if the first transistor or group of transistors is used for the design, determining whether the first transistor or group of transistors can be forward biased to operate in a high speed mode; and

if the first transistor or group of transistors can be forward biased to operate in a high speed mode and a programmable logic device power consumption specification and a programmable logic device routability specification permit, forward biasing the first transistor or group of transistors to operate in high speed mode.

90. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of logic elements, the method comprising:

evaluating whether a first logic element is used for a design implemented in the programmable logic device;

if the first logic element is not used for the design, searching for a second logic element that, if routed on routing that is proximal to the first

logic element, reduces leakage current across transistors that are located between routing wires associated with the first logic element and routing wires associated with the second logic element.

91. The method of claim 90, where the second logic element is selected by searching for a logic element whose output is substantially correlated to an output value of the first element.

92. The method of claim 90, further comprising replicating an output of the first logic element at the output of the second logic element.

93. The method of claim 90 further comprising replicating a portion of the routing of the first element so as to reduce total leakage current.

94. The method of claim 90, where the first logic element is known to have an unequal distribution of being in a ZERO output state and a ONE output state, and where the second logic element is selected on the basis of the second logic element favoring in its distribution of a ZERO output state and a ONE output state the same value as the value favored by the first logic element.

95. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of multiplexers, each of the multiplexers comprising a plurality of inputs, the method comprising:

where a programmable logic device speed specification and a programmable logic device

routability specification permit, minimizing the use of multiplexers that comprise one input that switches and the remaining inputs do not switch; and

maximizing the occurrence of multiplexers that comprise no inputs that switch.